What is claimed is:

1. A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove being formed to have a width-increased groove portion in said dielectric film as to expose a bottom surface of said semiconductor layer;

an impurity diffusion source buried in said width-increased groove portion of said groove to be contacted with said bottom surface of said semiconductor layer; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

2. The semiconductor device according to claim 1, wherein said groove is formed deep enough to reach the inside of said semiconductor substrate after penetration

through said dielectric film, and further comprising:

a trench capacitor formed under said dielectric film to have a storage electrode as half buried in said groove, for constitution of a DRAM cell together with said transistor.

3. The semiconductor device according to claim 2, wherein a buried strap for use as said impurity diffusion source is formed and buried in said width-increased groove portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film with the gate electrode of said transistor embedded to overlie said cap insulation film.

4. The semiconductor device according to claim 3, wherein said buried strap comprises a first strap buried on said storage electrode and a second strap stacked on the first strap and buried in said width-increased groove portion being in contact with said semiconductor layer only at the bottom surface thereof.

5. The semiconductor device according to claim 3, wherein said width-increased groove portion of said groove is formed to cover an entire range of a thickness of said dielectric film whereas the storage electrode of said capacitor is half buried in said width-increased groove portion with said buried strap being embedded on said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof.

6. The semiconductor device according to claim 2,

wherein said semiconductor layer is partitioned into a plurality of island-like element regions by an element isolating insulative film as formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said island-like element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of said transistor being continuously disposed along one direction and also with a bit line coupled to the second diffusion layer of said transistor being provided to cross said word line.

7. The semiconductor device according to claim 6, wherein said bit line is in contact with said second diffusion layer per each DRAM cell at a position adjacent to word lines at both ends of each said island-like element region, and wherein a body wire lead is formed to be contacted with said semiconductor layer across central part of said island-like element region for applying a fixed potential to said semiconductor layer.

8. The semiconductor device according to claim 2, wherein said semiconductor layer is partitioned into a plurality of island-like element regions by an element isolating insulative film as formed and buried with a depth failing to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said island-like element region to thereby constitute a DRAM cell array with a word line connected to the gate electrode of

said transistor being continuously disposed along one direction and also with a bit line coupled to the second diffusion layer of said transistor being provided to cross said word line.

9. A method of fabricating a semiconductor device comprising:

forming a groove in an element substrate having a semiconductor layer of a first conductivity type as insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, the groove being penetrating said semiconductor layer;

selectively etching said dielectric film exposed at said groove to form a width-increased groove portion for permitting exposure of a bottom surface of said semiconductor layer;

forming an impurity diffusion source buried in said width-increased groove portion said groove while letting said impurity diffusion source be in contact with only the bottom surface of said semiconductor layer;

forming and burying in said groove a gate electrode along with an underlying gate insulation film; and

forming in said semiconductor layer source and drain diffusion layers through impurity diffusion to a top surface and also impurity diffusion to the bottom surface by use of said impurity diffusion source.

10. A method of fabricating a semiconductor device comprising:

forming a groove in an element substrate having a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, the groove being deep enough to penetrate said semiconductor layer and said dielectric film and reach inside of said semiconductor substrate;

forming a capacitor by burying a storage electrode in said groove with a capacitor insulation film underlying the storage electrode;

etching said dielectric film exposed to a side face of said groove over said storage electrode to form a width-increased groove portion for permitting exposure of a bottom surface of said semiconductor layer;

burying an impurity doped strap in said width-increased groove portion of said groove as to overlap said storage electrode and to be contacted with said semiconductor layer only at said bottom surface;

burying a cap insulation film in said groove with said strap buried therein;

burying, after having formed a gate insulation film on a side face of said groove over said cap insulation film, a gate electrode of a transistor making up a DRAM cell along with said capacitor; and

forming source and drain diffusion layers of said transistor in said semiconductor layer, said source and drain diffusion layers being formed through impurity

diffusion to a top surface of said semiconductor layer and impurity diffusion to said bottom surface of said semiconductor layer by use of said strap, respectively.

11. The method according to claim 10, wherein said strap is buried to have a surface lower in level than the bottom surface of said semiconductor layer.

12. The method according to claim 10, further comprising:

burying, after having formed said source and drain diffusion layers, an element isolation insulative film in said semiconductor layer for partition of a plurality of island-like element regions each containing therein at least one DRAM cell;

forming a word line for common connection of gate electrodes of transistors aligned in a first direction; and

forming a bit line for common connection of drain diffusion layers of transistors aligned in a second direction transverse to said first direction.

13. The method according to claim 12, wherein said element isolation insulative film is formed deep enough to reach said dielectric film.

14. A method of fabricating a semiconductor device comprising:

forming a groove in an element substrate having a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, the groove being

deep enough to penetrate said semiconductor layer and said dielectric film and reach inside of said semiconductor substrate;

forming a capacitor by burying a storage electrode in said groove with a capacitor insulation film underlying the storage electrode;

burying a first strap doped with an impurity on said storage electrode of said groove;

etching said dielectric film being exposed at a side face of said groove over said first strap to form a width-increased groove portion for permitting exposure of a bottom surface of said semiconductor layer;

burying a second strap doped with an impurity in said width-increased groove portion of said groove to overlap said first strap and to be contacted with said semiconductor layer only at said bottom surface;

burying a cap insulation film in said groove with the second strap buried therein;

burying, after having formed a gate insulation film on a side face of said groove over said cap insulation film, a gate electrode of a transistor making up a DRAM cell together with said capacitor; and

forming source and drain diffusion layers of said transistor in said semiconductor layer, said source and drain diffusion layers being formed through impurity diffusion to a top surface of said semiconductor layer and impurity diffusion to said bottom surface of said

semiconductor layer by use of said second strap, respectively.

15. The method according to claim 14, wherein said second strap is buried to have a surface lower in level than the bottom surface of said semiconductor layer.

16. The method according to claim 14, further comprising:

burying, after having formed said source and drain diffusion layers, an element isolation insulative film in said semiconductor layer to partition said semiconductor layer into a plurality of island-like element regions each including at least one DRAM cell;

forming a word line for common connection of gate electrodes of transistors aligned in a first direction; and

forming a bit line for common connection of drain diffusion layers of transistors arrayed in a second direction transverse to said first direction.

17. The method according to claim 16, wherein said element isolation insulative film is formed deep enough to reach said dielectric film.

18. A method of fabricating a semiconductor device comprising:

forming a groove in an element substrate having a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed therebetween, said groove being deep enough to penetrate said semiconductor layer and said

dielectric film and reach inside of said semiconductor substrate;

etching said dielectric film exposed at a side face of said groove to form a width-increased groove portion for permitting exposure of a bottom surface of said semiconductor layer;

burying a storage electrode in said groove at a depth corresponding to mid part of said width-increased groove portion to form a capacitor;

burying an impurity doped strap in said width-increased groove portion to overlap said storage electrode and to be contacted with said semiconductor layer only at the bottom surface;

burying a cap insulation film in said groove to cover said strap;

burying, after having formed a gate insulation film on a side face of said groove over said cap insulation film, a gate electrode of a transistor making up a DRAM cell together with said capacitor; and

forming source and drain diffusion layers of said transistor in said semiconductor layer, said source and drain diffusion layers being formed through impurity diffusion to a top surface of said semiconductor layer and impurity diffusion to said bottom surface of said semiconductor layer by use of said strap, respectively.

19. The method according to claim 18, wherein said strap is buried to have a surface lower in level than the

bottom surface of said semiconductor layer.

20. The method according to claim 18, further comprising:

burying, after having formed said source and drain diffusion layers, an element isolation insulative film to partition said semiconductor layer into a plurality of island-like element regions each including at least one DRAM cell;

forming a word line for common connection of gate electrodes of transistors aligned in a first direction; and

forming a bit line for common connection of drain diffusion layers of transistors arrayed in a second direction transverse to said first direction.